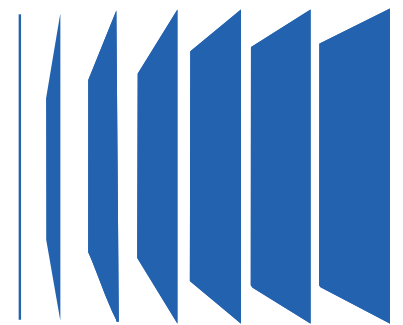




Taiwan-Europe Semiconductor Short-term Training Program 2025



Program 1 Jun 30- Jul 25

Design Trends and Technological Transformations in Semiconductor
for 1 week: **National Taiwan University**

or Emerging Trends and Future Directions in Semiconductor Technology and IC Design

for 1 week: **National Cheng Kung University**
&

Practical Training for 3 weeks:
Taiwan Semiconductor Research Institution

Program 2 Jul 7- Aug 1

Practical Training for 4 weeks:
Taiwan Semiconductor Research Institution



Registration

July, 2025

Program Introduction

This summer, we are offering two 4-week training programs to choose from.

The first program runs from June 30 to July 25, starting with one week of classes at either National Taiwan University (NTU) or National Cheng Kung University (NCKU), followed by three weeks of hands-on training at TSRI.

The second program runs from July 7 to August 1 and will be conducted entirely at TSRI. During the final week, participants will work on a project, applying the skills they have acquired.

Program Timeline

Program 1

Program 2

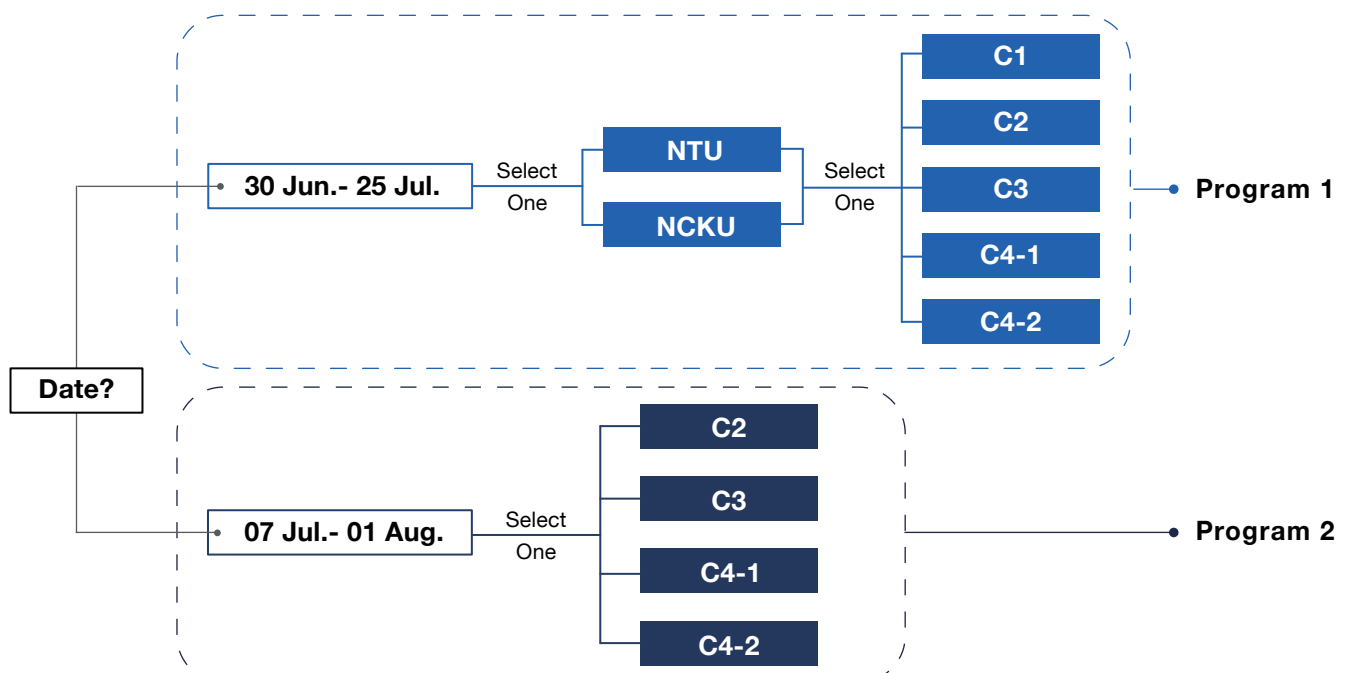
W1 Jun. 30	W2 Jul. 07	W3 Jul. 14	W4 Jul. 21	W5 Jul. 28
NTU / NCKU	TSRI: C1 / C2 / C3 / C4-1 / C4-2			
	TSRI: C2 / C3 / C4-1 / C4-2			TSRI: Project

- C1** Cell-based IC Design, Implementation and Verification & SoC FPGA Prototyping
- C2** Analog Design Essential (TSRI, Tainan)
- C3** Practical Power Management IC Design (TSRI, Tainan)
- C4-1** Full-Custom IC Design & CMOS MEMS IC Design
- C4-2** Full-Custom IC Design & Silicon Photonic IC Design for High-Speed Applications

How to Enroll?

Each course has a limited number of spots available. Please register early to secure your place.

The organizer reserves the right of final decision.



2025 Taiwan-Europe Semiconductor Short-term Training Program:

Design Trends and Technological Transformations in Semiconductor

Target Audience:

Junior, senior, and graduate students with a VLSI course or other related courses grade of A- or higher.

NTU Courses

	Morning Session	Afternoon Session
JUN 29	Arrival & Check-in	
JUN 30	<ul style="list-style-type: none"> - Campus Tour Orientation - Opening Ceremony Welcome Lunch 	The History and Future of Chip Design and Manufacturing (Chip Wars)
JUL 01	Integrated Circuit Process / Transistors / Science	Project Discussion
JUL 02	Integrated Circuit Design	Project Discussion
JUL 03	Electronic Design Automation	The Future of Semiconductor Electronics
JUL 04	NTU Museum / NTU NEMS Research Center	Project Discussion / Rehearsal
JUL 05	<ul style="list-style-type: none"> - Hotel Check-out - Final Presentation Closing Ceremony - Farewell Lunch 	Departure to TSRI

** Schedule is subject to change

2025 Taiwan-Europe Semiconductor Short-term Training Program :

Emerging Trends and Future Directions in Semiconductor Technology and IC Design

Target Audience:

Junior, senior, and graduate students with a VLSI course or other related courses grade of A- or higher.

NCKU Courses

	Morning Session	Afternoon Session
JUN 29	Arrival & Check-in	
JUN 30	Opening Ceremony & Welcome Lunch	NCKU Campus Tour
JUL 01	Cultural Tour of Tainan	Integrated Circuit Design Overview
JUL 02	Digital IC Design	Analog IC Design
JUL 03	IC Design Testing	IC Design Verification
JUL 04	Advanced Device for Next Generation Chip	Project Discussion
JUL 05	<ul style="list-style-type: none"> - Hotel Check-out - Group Presentation & Closing Ceremony 	Departure to TSRI

** Schedule is subject to change

Overall of Courses in TSRI

C1 Cell-based IC Design, Implementation and Verification & SoC FPGA Prototyping

Target Audience:

Undergraduate (junior or above), master's, and PhD students in electronics, electrical engineering, or related fields, with interest in analog or mixed-signal IC design. Priority given to those who have completed an analog circuit design-related course with a grade of A- or above.

Jul 7 - July 11

Day 1

- Opening Ceremony
- Verilog

Day 2

Verilog

Day 3

Verilog

Day 4

Logic synthesis with Design Compiler

Day 5

Logic synthesis with Design Compiler

Jul 14 - July 18

Day 6

Logic synthesis with Design Compiler

Day 7

Physical design and verification with Innovus

Day 8

Physical design and verification with Innovus

Day 9

Physical design and verification with Innovus

Day 10

SoC FPGA Prototyping (Hardware)

Jul 21 - July 25

Day 11

SoC FPGA Prototyping (Hardware)
SoC FPGA Prototyping (Firmware)

Day 12

SoC FPGA Prototyping (Firmware)

Day 13

SoC FPGA Prototyping (Firmware)

Day 14

Company visiting

Day 15

MOFA Closing Ceremony

Overall of Courses in TSRI

C2 Analog Design Essential

Target Audience:

Undergraduate (junior or above), master's, and PhD students in electronics, electrical engineering, or related fields, with interest in analog or mixed-signal IC design. Priority given to those who have completed an analog circuit design-related course with a grade of A- or above.

Jul 7 - July 11

Day 1

- Opening Ceremony
- Introduction IC Design Flow

Day 2

- Fundamental of Process, Device & Modeling:
- 1) Process
 - 2) Device
 - 3) Device Model

Day 3

- Operational Amplifier:
- 1) Concept
- 2) Stability

Day 4

- Operational Amplifier:
- 1) Concept
 - 2) Specifications

Day 5

- Operational Amplifier:
- 3) Architecture
- 4) Single-stage OTA design

Jul 14 - July 18

Day 6

- Operational Amplifier:
- 3) Stability
 - 4) Two-stage OTA design

Day 7

- Operational Amplifier:
- 5) Bias Circuit
 - 6) Common-Mode Feedback Design

Day 8

- Operational Amplifier:
- 7) Thermal Noise
 - 8) Flicker Noise

Day 9

- Operational Amplifier:
- 9) CDS
 - 10) Chopper

Day 10

- Process/Design related company visiting

Jul 21 - July 25

Day 11

- EDA Tools For Circuit Design:
- 1) PDK
 - 2) Virtuoso

Day 12

- EDA Tools For Circuit Design:
- 3) Hspice
 - 4) Simulation

Day 13

- Non-Ideal Effect:
- 1) Process Variation
 - 2) PVT

Day 14

- Layout:
- 1) Concept
 - 2) Layout Dependent Effect

Day 15

- MOFA Closing Ceremony

Jul 28 - Aug 1

Day 16-20

- Project: Hybrid-Compensated Two-Stage OTA Design

Overall of Courses in TSRI

C3 Practical Power Management IC Design

Target Audience:

Undergraduate (junior or above), master's, and PhD students in electronics, electrical engineering, or related fields, with interest in power management IC design. Priority given to those who have completed have completed VLSI design-related and power systems circuit courses with a grade of A- or higher.

Jul 7 - July 11

Day 1

- Opening Ceremony
- I. Full-Custom IC Design Flow-Introduction

Day 2

- I. Full-Custom IC Design Flow-Circuit Design and Simulation Tools

Day 3

- I. Full-Custom IC Design Flow-
 - 1) Basic Layout Concept and Layout Tools
 - 2) Layout Verification

Day 4

- I. Full-Custom IC Design Flow-Lab: A Non-Overlapping Clock Generator

Day 5

- II. Circuit Implementation with BCD Process-Introduction

Jul 14 - July 18

Day 6

- II. Circuit Implementation with BCD Process-High Voltage Circuit Design Concept

Day 7

- II. Circuit Implementation with BCD Process-Protection Mechanisms

Day 8

- II. Circuit Implementation with BCD Process-HV Linear Regulator Design

Day 9

- II. Circuit Implementation with BCD Process- Lab: A HV Linear Regulator

Day 10

- Process/Design related company visiting

Jul 21 - July 25

Day 11

- III. Integrated Power Stage Circuit Design-Power Stage:
 - 1) Parasitic effect
 - 2) Switch Behavior

Day 12

- III. Integrated Power Stage Circuit Design-Gate Driver
 - 1) Introduction
 - 2) DC Characteristics
 - 3) Driving Strength

Day 13

- III. Integrated Power Stage Circuit Design-Dead Time Generation:
 - 1) Architecture
 - 2) Power Losses

Day 14

- III. Integrated Power Stage Circuit Design-Level Shifter
 - 1) Architecture
 - 2) Switching Behavior

Day 15

- MOFA Closing Ceremony

Jul 28 - Aug 1

Day 16-20

- Project: Chip Design for Step-Down Switching Regulators

Overall of Courses in TSRI

C4-1 Full-Custom IC Design & CMOS MEMS IC Design

Target Audience:

Undergraduate (junior or above), master's, and PhD students in electronics, electrical engineering, mechanical engineering, or related fields, with interest in microelectromechanical systems (MEMS). Priority given to those who have completed a VLSI Design-related course with a grade of A- or above.

Jul 7 - July 11

Day 1

- Opening Ceremony
- Full-Custom IC Design Overview

Day 2

- Introduction of U18 FDK
- Circuit Simulation with ADE and Spectre

Day 3

- Fundamentals of Full-Custom Cell Design and Simulation
- Layout Skill and Implementation

Day 4

- Layout Verification (DRC, LVS and LPE) and Debugging

Day 5

- Project Layout (DRC, LVS and LPE)
- Finish the Project Layout (Comparison between Pre-Sim and Post-Sim)

Jul 14 - July 18

Day 6

- Preview of MEMS Technology
- TSRI CMOS MEMS Process
- Lab: Design accelerometer in simulation version

Day 7

- Applications of CMOS MEMS Technology
- Characterizing the MEMS Devices
- Lab: Design accelerometer in tape-out version

Day 8

- Applications of Accelerometer
- Design and Architecture of Accelerometer
- Simulation by CoventorWare

Day 9

- TSRI CMOS MEMS Process Flow and Design Rules
- TSRI CMOS MEMS MPW
- The MEMS Measuring Instruments in TSRI
- Visit to the MEMS Measurement Laboratory

Day 10

- Introduction of Capacitive Sensing Readout Circuit/IP User Guide
- Lab: G-sensor readout circuit simulation and integrate MEMS with readout circuit

Jul 21 - July 25

Day 11

- Application and Working Principle of Resonator
- Design and Architecture of Resonator
- Lab: Design resonator in simulation and tape-out version

Day 12

- Introduction and Design of TIA Readout Circuit
- Lab: Simulation of TIA Circuit

Day 13

- Company visiting

Day 14

- TIA Layout Guideline/Layout Verification
- Combine MEMS and Readout Circuit
- Lab: Design TIA for Simulation and Layout

Day 15

- MOFA Closing Ceremony

Jul 28 - Aug 1

Day 16-20

- Introduction and Practical Operation of MEMS Laboratory
- Project: Design of sub-MHz resonator/oscillator (MEMS Resonator + TIA Read Circuit)
 - *Design a CMOS MEMS Resonator
 - *Design of a Transimpedance Amplifier
 - *Integration of CMOS MEMS Oscillator

Overall of Courses in TSRI

C4-2 Full-Custom IC Design & Silicon Photonic IC Design for High-Speed Applications

Target Audience:

This course is open to undergraduate and graduate students from departments such as Electrical Engineering, Electronics, Photonics, Physics, Chemistry, or other related disciplines. Applicants should have a minimum academic performance of A- (or equivalent) or above in their relevant coursework.

Jul 7 - July 11

Day 1

- Opening Ceremony
- Full-Custom IC Design Overview

Day 2

- Introduction of U18 FDK
- Circuit Simulation with ADE and Spectre

Day 3

- Fundamentals of Full-Custom Cell Design and Simulation
- Layout Skill and Implementation

Day 4

- Layout Verification (DRC, LVS and LPE) and Debugging

Day 5

- Project Layout (DRC, LVS and LPE)
- Finish the Project Layout (Comparison between Pre-Sim and Post-Sim)

Jul 14 - July 18

Day 6

- Introduction
- Photonics processing, Si straight waveguide

Day 7

- Si bending, Grating coupler and edge coupler

Day 8

- Modulator theory and design

Day 9

- Performance Analysis of the Optical Modulator

Day 10

- Silicon photonics testing: coupling method and eye diagram testing

Jul 21 - July 25

Day 11

- Photodetector theory and design

Day 12

- Optical PAM4 circuit design and simulation

Day 13

- Anritsu company visiting

Day 14

- Optical PAM4 circuit layout
- Optical PAM4 circuit Design Rules Checking

Day 15

- MOFA Closing Ceremony

Jul 28 - Aug 1

Day 16-20

- Design project: High Extinction Ratio Optical PAM4 Circuit

July, 2025

Information

Participant Support

- Each participant will receive a daily allowance of NTD 1,000.
- The round-trip tickets for participants will be arranged by the relevant Taiwan Representative Office.
- Accommodation in Taiwan will be arranged by the host organization.

Application Procedure

Applicants are required to complete the online application form and submit hard copies of the following documents, either by post or in person, to the relevant Taiwan Representative Office in Europe by May 12, 2025 :

- A copy of the passport bio page
- Academic transcript
- Certificate of education
- 2 passport-size photos



Registration

Contact Information

Please refer to the contact details of the training organizers and the seven Taiwan Representative Offices in Europe below.

Training Organizers

01 International College at National Taiwan University

Rita Huang
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02 NCKU's Academy of Innovative Semiconductor and Sustainable Manufacturing

Kacie Liu
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03 Taiwan Semiconductor Research Institute

Email: tsri-tc@nlar.org.tw

Taiwan Representative Offices In Europe

01 Taipei Economic and Cultural Office, Prague

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02 The Taiwanese Representative Office in Lithuania

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03 Taipei Representative Office, Bratislava

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05 Taipei Representative Office ,Budapest, Hungary

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06 Taipei Representative Office in Greece

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